(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 178 388 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
06.02.2002 Bulletin 2002/06

(21) Application number: **00830560.9**

(22) Date of filing: **04.08.2000**

(51) Int Cl.[7]: **G06F 1/025**, H03L 7/00, H03M 1/68 // H03M1/82

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(71) Applicant: **STMicroelectronics S.r.l.**
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Grosso, Antonio**
  20139 Milano (IT)
- **Botti, Edoardo**
  27029 Vigevano (PV) (IT)

(74) Representative: **Mittler, Enrico et al**
c/o Mittler & C. s.r.l., Viale Lombardia, 20
20131 Milano (IT)

(54) PCM/PWM converter with PWM power amplifier

(57) A PWM power amplifier is herein described comprising at least one PCM/PWM converter (2, 3, 20, 30) which is fed by PCM digital input signals (Ip, Is) and produces PWM digital output signals (Op, Os, Opn, Ops), and at least one power amplification final stage (10, 101, 102) of the PWM digital output signals (Op, Os, Opn, Ops) by said at least one PCM/PWM converter (2, 3, 20, 30). At least one PCM/PWM converter (2, 3, 20, 30) comprises a counter (up-counter, up-down counter) fed with at least one clock signal (E) produced by a clock generator device (5) and comprising a digital comparator (8) suitable for comparing said PCM digital input signals (Ip, Is) of at least one PCM/PWM converter (2, 3, 20, 30) with a digital comparison signal (B, Z) produced by the counter (up-counter, up-down counter) and producing in output the PWM digital signals (Op, Os, Opn, Ops). The clock generator device (5) comprises a pulse generator device (6) and an oscillator (7); the pulse generator device (6) receives a signal at a frequency (Fin*k) which is equal to the frequency of the PCM digital input signals (Ip, Is) of said at least one PCM/PWM converter (2, 3, 20, 30) and produces in output reset pulses (IR). The reset pulses (IR) are sent in input to the oscillator (7) which produces in output said at least one clock signal (E).

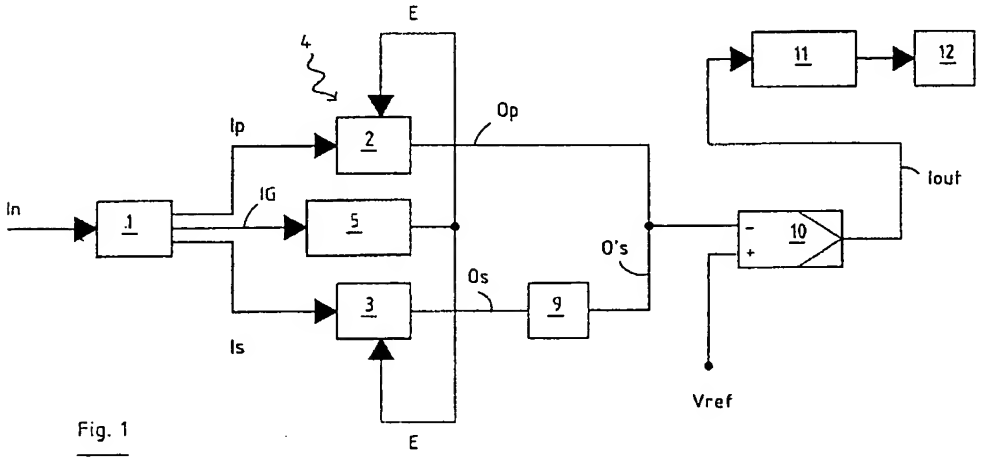

Fig. 1

EP 1 178 388 A1

Description

[0001] The present invention is a PWM power amplifier, specifically a digital input PWM power amplifier.

[0002] The general trend to reduce energy consumption and the weight and overall dimension represented by heatsinks has stimulated the request of equipment manufacturers for audio power amplifiers with greater efficiency than "AB" class amplifiers.

[0003] To meet these requests audio amplifiers in class D have been proposed which comprises a DC-AC converter circuit which produces a pulse width modulated (PWM) output signal; said PWM signal in turn drives power switches which drive a load provided with a passive filter for the reconstruction of the amplified audio signal.

[0004] A single output amplifier with analogue input and PWM output (class-D amplifier) is described in the article "Analysis of a quality class-D amplifier", F.A. Himmelstoss, et al., I.E.E.E. Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996.

[0005] Widening interest in the digital processing of signals has lead to the manufacture of power amplifiers with digital input instead of analogue input. Said digital input power amplifiers include PCM/PWM converters capable of converting a PCM digital signal into a PWM digital signal, a final stage of power amplification receiving the PWM digital signal and generating an amplified PWM analogue output signal that drives a load provided with a passive filter for the reconstruction of the amplified audio signal. The PCM/PWM converter comprises a counter fed by a clock signal and generating digital comparison words and a digital comparator receiving the digital comparison words through a first input and the PCM digital signal through a second input and producing a digital PWM signal in output.

[0006] In a power amplifier of the above type, the device for generating the clock signal needed for the PCM/PWM conversion of the digital signal in input is typically made up of a PLL clock generator (phase locked) which, in per se known way, consists of a loop structure comprising a phase comparator, a filter, a voltage controlled oscillator, a frequency divider.

[0007] A PLL clock generator nevertheless presents a complex structure and is affected by various types of noise above all in virtue of the presence of the phase comparator.

[0008] In view of the state of the technique described, the object of the present invention is to present a PWM power amplifier provided with a clock generator that at least partially eliminates the above mentioned inconveniences.

[0009] In accordance with the present invention, said object is reached by means of a PWM power amplifier comprising at least one PCMIPWM converter that is fed with PCM digital input signals and produces PWM digital output signals, and at least one final stage of power amplification of the PWM digital signals in output from said at least one PCM/PWM converter, said at least one PCM/PWM converter comprising a counter fed with at least one clock signal produced by a clock generator device and comprising a digital comparator suitable for comparing said PCM digital input signals of said at least one PCM/PWM converter with a digital comparison signal produced by said counter and producing said PWM digital signals in output, characterized in that said clock generator device comprises a pulse generator device and an oscillator, said pulse generator device receiving a signal at a frequency that is equal to the frequency of said PCM digital input signals of said at least one PCM/PWM converter and producing reset pulses in output , said reset pulses being sent in input to said oscillator producing said at least one clock signal in output .

[0010] Thanks to the present invention a PWM power amplifier can be produced provided with a clock generator which has a simpler circuit than the known clock generator devices and which is less effected by noise in comparison with the same known devices.

[0011] The characteristics and advantages of the present invention will appear evident from the following detailed description of embodiments thereof, illustrated as non-limiting examples in the enclosed drawings, in which:

Figure 1 is a block diagram of the basic structure of the PWM power amplifier according to a first embodiment of the present invention;

Figure 2 is a block diagram of the clock generator of the power amplifier in figure 1;

Figure 3 shows the waveforms of the clock generator in Figure 2;

Figure 4 is a circuit diagram of the oscillator of the clock generator in Figure 2;

Figure 5 is a diagram of the internal structure of each of the two PCM/PWM single ramp converters in Figure 1;

Figure 6 shows the operating waveforms of a PCM/PWM single ramp converter;

Figure 7 is a block diagram of the basic structure of a power amplifier according to a second embodiment of the invention characterized by the use of PCM/PWM double ramp converters;

Figure 8 shows the internal structure of a PCM/PWM double ramp converter;

Figure 9 shows the operating waveforms of the PCM/PWM double ramp converter in Figure 8;

Figure 10 is a block diagram of the basic structure of a power amplifier according to a third embodiment of the invention;

Figure 11 is a block diagram of the basic structure of a power amplifier according to a fourth embodiment of the invention;

Figure 12 is a block diagram of the basic structure of a power amplifier according to a fifth embodiment of the invention;

Figure 13 is a block diagram of the basic structure

of a power amplifier according to a sixth embodiment of the invention.

[0012] With reference to Figure 1 a power amplifier according to the first embodiment of the present invention is shown, in which initially a digital signal In with pulse code modulation (PCM) with a number M of bits at bit frequency Fin is sent in input to a block 1, where it is converted with oversampling techniques and noise shaping into a digital signal with a number N of bits lower than the number of bits of the digital signal In (M>N) and with a multiple bit frequency, Fin*k, compared to the bit frequency Fin of the digital signal In.

[0013] The N bits that compose the signal in output from the block 1 of oversampling and noise shaping are subdivided into two distinct buses, a first bus that transmits a first number P of more significant bits (MSB) and a second bus transmitting a number S of less significant bits (LSB), so as to form respective digital signals Ip and Is at the frequency Fin*k.

[0014] The digital signals Ip and Is are sent in input to two PCM/PWM converters, respectively the digital signal Ip is in input to the PCM/PWM converter 2 while the digital signal Is is in input to the PCM/PWM converter 3. The PCM/PWM converters 2 and 3 are part of a block 4 of conversion of digital data at pulse code modulation (PCM) into digital data at pulse width modulation (PWM) which also comprises a clock generator 5 suitable for producing a signal E at clock frequency Fclock necessary for the PCM/PWM conversion of the digital data.

[0015] The subdivision of the bits of the N bit digital signals into which the PCM digital signals in input In at M bit are reorganized, enables the use of not exceedingly high clock frequencies Fclock in the block 4. In fact, wanting to transform into a PWM signal a PCM signal at 16 bits at 44.1kHz without a noticeable deterioration of the signal/noise ratio, a sampling clock equal to $44100*2^{16}=2.8GHz$ would be necessary, which is a value that could not be proposed for the present integrated circuits.

[0016] Another problem overcome by the subdivision carried out consists in the fact that the commutation frequency of the PWM signal in output, which in the example taken into consideration is 44.1kHz, would be too close to the maximum frequency to reproduce (generally in an audio system at about 20kHz), causing problems of harmonic distortion, frequency linearity and signal residues at commutation frequency downstream from the low-pass reconstruction filter.

[0017] If a commutation frequency of the PWM signal is required far enough from the audio band and considering the fact that normally the commutation frequency of the PWM amplifiers is between 100kHz and 500kHz, for example in the case considered about $44100*8=352.8kHz$, and opting for a number of more significant bits (MSB) P=6 and a number of less significant bits (LSB) S=6, the clock frequency Fclock will be $352800*2^6=22.57MHz$, which can be handled with the present technologies used for the manufacture of integrated circuits.

[0018] The clock generator 5 comprises a reset pulse generator 6 and an oscillator 7, as can be seen in Figure 2. The reset pulse generator 6, which can be formed for example by a one-shot multivibrator, has a square wave IG input signal at frequency Fin*k, and generates an IR pulse output signal where the pulses are generated at each variation of the IG signal, as can be seen Figure 3. The signal IR is sent to an input R of the oscillator 7 which produces in output (OUT) the required clock signal E at frequency Fclock.

[0019] In Figure 4 a possible implementation of the oscillator 7 is shown. The input R of the oscillator 7 is placed on the gate terminal of a MOS transistor Mr which has the source grounded and the drain connected to a terminal of a capacitor C1 having the other terminal grounded, to the gate terminals of the MOS transistors M1, M2 being part of a first inverter, to the output OUT of the oscillator 7. The transistors M1, M2 have the source terminals connected to suitable current generators and the drain terminals connected to a terminal of a capacitor C2 which has the other terminal grounded and connected to the gate terminals of two MOS transistors M3, M4 being part of a second inverter. The transistors M3, M4 have the source terminals connected to suitable current generators and the drain terminals connected to a terminal of a capacitor C3 which has the other terminal grounded and connected to the gate terminals of two MOS transistors M5, M6 being part of a third inverter. The transistors M5, M6 have the source terminals connected to suitable current generators and the drain terminals connected to the output OUT. The bulk terminals of the transistors Mr, M2, M4, M6 are grounded while the bulk terminals of the transistors M1, M3, M5 are connected to a voltage supply Vcc. The transistor Mr brings the clock signal E at frequency Fclock to a low value when an impulse IR is present on its gate terminal, as can be seen in Figure 3; in this manner the oscillator 7 can be reset.

[0020] The functional block diagram and the functional waveforms valid for each of the two PCM/PWM converters 2 and 3 used in the PWM power amplifier in Figure 1 are shown in Figures 5 and 6; for simplicity only the PCM/PWM converter 2 will be described hereinafter.

[0021] Said PCM/PWM converter 2 is of the single ramp B type obtained by means of an up-counter, cyclic or resettable, powered by the clock signal E at frequency $Fclock=(Fin*k)*2^P$, that is equal to the product of the frequency of the signal Ip in input to the converter 2 by the power in base two of the number of bits P which form the signal Ip; the clock signal E is obtained by means of the clock generator 5 previously described. The ramp B signal is compared with the PCM digital signal Ip by a digital comparator 8; the result of the comparison is the PWM digital signal Op in output from the converter 2 whose duty-cycle is function of the MSB input data and whose frequency is Fin*k. In the same manner the PWM

digital signal Os in output from the converter 3 will have a duty-cycle which depends on the LSB input data and whose frequency is Fin*k.

[0022] The PWM digital signal Os in output from the converter 3 is attenuated in the block 9 by a ratio equivalent to the power in base two of the number S of bits transmitted to the input of the same converter thereby obtaining a signal O's=Os/(2^S). The signals Op and O's are summed at the inverting node of a power amplification final block 10 (the output stage of the PWM power amplifier) which is the power amplification module functioning in class D described and illustrated in the European patent application No. 1001526. A reference voltage Vref is connected to the non-inverting node of the block 10.

[0023] The PWM digital signal Op produced by the PCM/PWM converter 2 drives the output stage 10 determining its commutation frequency. The PWM digital signal O's drives the block 10 with a weight reduced by $1/2^S$; in this manner the signal O's modulates the PWM signal Iout in output from block 10 correcting its non-linearity and attenuating the noise introduced by the quantization to a reduced number P of bits of the PWM digital signal Op.

[0024] The amplified PWM signal Iout is sent in input to a low-pass filter 11 which provides for the reconstruction of the starting audio signal; the signal in output from filter 11 will be sent to a load 12 made up for example by a loudspeaker.

[0025] Hereinafter other embodiments of the present invention will be described in which the elements equal to the first or to other embodiments will have the same references.

[0026] In Figures 7-9 a PWM power amplifier according to a second embodiment is described which differs from the first embodiment in the use of the PCM/PWM double ramp converters instead of single ramp converters; in this manner the frequency of the PWM signals produced in output from the two PCM/PWM 2 and 3 converters is halved compared to the Fin*k frequency of the digital signals Ip an Is in input to the converters 2 and 3.

[0027] The functional block diagram and the functional waveforms valid for each of the two PCM/PWM double ramp converters 2 and 3 used in the PWM power amplifier in Figure 1 are shown in Figures 8 and 9; for simplification only the PCM/PWM converter 2 will be described hereinafter.

[0028] Said PCM/PWM converter 2 is of the double ramp Z type obtained by means of an up-down counter, cyclic or resettable, powered both with the signal of clock E at frequency Fclock=(Fin*k)*2^P, that is equal to the product of the frequency of the signal Ip in input to the converter 2 by the power in base two of the number of bits P that form the signal Ip (the clock signal E is obtained by means of the clock generator 5 previously described), and with a second clock signal D at frequency Fup/down (produced by a clock generator different from generator 5) with the frequency Fup/down=Fin*k which synchronizes the ramp inversions. The double ramp signal Z is compared with the PCM digital signal Ip by a digital comparator 8; the result of the comparison is the PWM digital signal Op in output from converter 2 whose duty-cycle is function of the MSB input data and whose frequency is Fin*k/2. In the same manner the PWM digital signal Os in output from converter 3 will have a duty-cycle which depends on the LSB input data and whose frequency is Fin*k/2.

[0029] The PWM digital signal Os in output from converter 3 is attenuated in block 9 in a ratio equivalent to the power in base two of the number S of bits transmitted to the input of the sane converter obtaining a signal O's=Os/(2^s). The signals Op and O's are summed at the inverting node of the power amplification final block 10.

[0030] The double ramp converters enable the performance of the amplifier to be improved from the point of view of the signal/noise ratio and of the distortion compared to the use of single ramp converters.

[0031] The block diagram of a PWM power amplifier according to a third embodiment of the invention is shown in Figure 10, differing from the second embodiment previously described only in the presence of an output which is no longer single but of bridge type, using two push-pull driven output stages 101 and 102 (with relative low-pass filters 111 and 112). The signals Op and O's are summed at the inverting node of the first output stage 101 while the signals Opn and O'sn (the signal O'sn is the signal Osn attenuated by block 9), which are respectively signals Op and O's negated, are summed at the inverting node of the output second stage 102. The output signals of the two stages 101 and 102 I'out and I"out are sent to the respective low-pass filters 111 and 112 and the output signals of the filters drive the load 12.

[0032] Figure 11 shows the block diagram of a PWM power amplifier according to a fourth embodiment of the invention which differentiates from the third embodiment previously described in that it provides for a double ramp conversion both for the signals Ip and Is and for the signals Ipn and Isn, which are the signals Ip and Is negated, by means of further double ramp PCM/PWM converters 20 and 30, similar to the converters 2 e 3, which supply in output the signals Opn and Osn. In said case the output of the PWM power amplifier is of the phase shift bridge type and presents a more complex architecture than that in Figure 10 but is capable of giving higher performance, as is described in detail and illustrated in the European patent application No. 1001526

[0033] Figure 12 shows the block diagram of a PWM power amplifier according to a fifth embodiment of the invention which differentiates from the fourth embodiment previously described in that the signals Opn and Osn in output from the PCM/PWM converters 20 and 30 derive not from inverted digital signals Ipn and Isn but by inverting the clock signal D at frequency Fup/down of the up-down counters of the converters 20 and 30, such as to generate triangular signals in counter-phase

between each other.

[0034] Figure 13 shows the block diagram of a PWM power amplifier according to a sixth embodiment of the invention which differentiates from the fifth embodiment previously described because the PWM digital signals Op and Opn are summed to twice the respective signals O's1 and O'sn1 which are the signals O's and O'sn at double frequency compared to the frequency of the signals Op and Opn, at the respective inverting nodes of the two output stages 101 and 102.

[0035] The advantages of said embodiment lie both in the fact that the correction signal (relative to the signals Os and Osn) can be added, subtracted or can also not influence the main drive signal (relative to the signals Op and Opn), and in the fact that the correction signal does not contain tones at PWM commutation frequency or in its proximity (the tones of a band of 20kHz around a commutation frequency are returned to base band causing an increase in distortion or noise).

[0036] In the embodiments illustrated in the Figures the blocks 9 and 200 can be constituted by simple resistors or by current generators controlled by the output logic signal of the respective PCM/PWM converters.

[0037] The frequency of the oscillator 7 of the clock generator 5 can be varied by continuously changing its characteristics; the consequence is a continuous variation of the width of the output signal of the PWM amplifier due to the variable gain of the PCM/PWM conversion block 4.

[0038] In all the embodiments previously described the clock signal E at frequency Fclock is produced by the generator 5 of Figure 2.

Claims

1. PWM power amplifier comprising at least one PCM/PWM converter (2, 3, 20, 30) which is fed by PCM digital input signals (Ip, Is) and produces PWM digital output signals (Op, Os, Opn, Ops), and at least one final stage (10, 101, 102) of power amplification of the PWM digital signals (Op, Os, Opn, Ops) in output from said at least one PCM/PWM converter (2, 3, 20, 30), said at least one PCM/PWM converter (2, 3, 20, 30) comprising a counter (up-counter, up-down counter) fed with at least one clock signal (E) produced by a clock generator device (5) and comprising a digital comparator (8) suitable for comparing said PCM digital input signals (Ip, Is) of said at least one PCM/PWM converter (2, 3, 20, 30) with a digital comparison signal (B, Z) produced by said counter (up-counter, up-down counter) and producing in output said digital signals PWM (Op, Os, Opn, Ops), **characterized in that** said clock generator device (5) comprises a pulse generator device (6) and an oscillator (7), said pulse generator device (6) receiving a signal at a frequency (Fin*k) equal to the frequency of said PCM digital input signals (Ip, Is) of said at least one PCM/PWM converter (2, 3, 20, 30) and producing in output reset pulses (IR), said reset pulses (IR) being sent in input to said oscillator (7) producing in output said at least one clock signal (E).

2. Amplifier according to claim 1, **characterized in** fact it comprises an oversampling and noise shaping block (1) receiving first PCM digital input signals (In) organized in words with a given number of bits (M) and at a given frequency (Fin) and producing in output second PCM digital signals (Ip, Is) organized in words composed of a number of bits (N) lower than said given number of bits (M) and at a multiple frequency (Fin*k) with respect to said given frequency (Fin) of the first PCM digital input signals (In), said second PCM digital signals (Ip, Is) being the PCM digital signals in input to said at least one PCM/PWM converter (2, 3, 20, 30).

3. Amplifier according to claim 2, **characterized in that** it comprises a first bus suitable for transmitting first digital data PCM (Ip) containing a first number (P) of more significant bits (MSB) of said second PCM digital signals (Ip, Is) and a second bus suitable for transmitting second PCM digital data (Is) containing a second number (S) of less significant bits (LSB) of said second PCM digital signals (Ip, Is), and **characterized in that** it foresees a first (2, 20) and a second (3, 30) PCM/PWM converter fed respectively by said first (Ip) and second (Is) PCM digital data and producing in output respectively a first (Op, Opn) and a second (Os, Osn) PWM signal.

4. Amplifier according to claim 3, **characterized in that** said second signal PWM (Os, Osn) is previously attenuated by a ratio equivalent to the power in base two of the second number (S) of less significant bits (LSB) transmitted by said second bus to the input of said second PCM/PWM converter (3, 30) and is summed to said first signal PWM (Op, Opn) at an inverting node (-) of said at least one power amplification final stage (10, 101, 102) of the amplifier.

5. Amplifier according to claim 1, **characterized in that** said at least one clock generator (5) produces a clock signal (E) whose frequency (Fclock) equals the product of the frequency (Fin*k) of the bits of the PCM digital signals (Ip, Is) in input to said at least one PCM/PWM converter (2, 3, 20, 30) by the power in base two of the number of bits (P, S) of said PCM digital signals (Ip, Is) in input to at least one PCM/PWM converter (2, 3, 20, 30), said counter (up-counter, up-down counter) fed by said at least one clock signal (E) generating a digital comparison output signal (B, Z) composed of said number of bits (P, S) in the form of at least one ramp of digital val-

ues at an identical or halved frequency compared to said frequency (Fin*k) of bits of the PCM digital signals (Ip, Is) in input to the at least one PCM/PWM converter (2, 3, 20, 30).

6. Amplifier according to claim 5, **characterized in that** said digital comparison signal (B) of said at least one PCM/PWM converter (2, 3, 20, 30) is in the form of a succession of upward ramps of digital values at a frequency identical to said frequency (Fin*k) of bits of the PCM digital signals (Ip, Is) in input to at least one PCM/PWM converter (2, 3, 20, 30).

7. Amplifier according to claim 5, **characterized in that** said at least one PCM/PWM converter (2, 3, 20, 30) is a double ramp type, said counter (up-down counter) being of the up/down type, having in input a ramp inversion signal (D) and generating in output a digital comparison signal (Z) composed by the number of bits (P, S) of said PCM digital signals (Ip, Is) in input to at least one PCM/PWM converter (2, 3, 20, 30) under the form of a succession of up and down ramps at a halved frequency (Fin*k/2) compared to the frequency of the PCM digital signals (Ip, Is) in input to said at least one PCM/PWM converter (2, 3, 20, 30).

8. Amplifier according to the claims 1 or 4, **characterized in that** it foresees a single power amplification final stage (10).

9. Amplifier according to the claims 1 or 4, **characterized in that** it foresees two identical power amplification final stages (102, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input of said two final stages is made by inverting the PWM digital signal (Op, Os) in output from said at least one PCM/PWM converter (2, 3).

10. Amplifier according to the claims 1 or 4, **characterized in that** it foresees two identical power amplification final stages (101, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input (-) of said two final stages (101, 102) is made by duplicating said at least one PCM/PWM converter (2, 3) and inverting the PCM digital signals (Ip, Is) in input to said at least two PCM/PWM converters (2, 3).

11. Amplifier according to the claims 1 and 4, **characterized in that** said at least one clock generator (5) produces a clock signal (E) whose frequency (Fclock) equals the product of the frequency (Fin*k) of the bits of the PCM digital signals (Ip, Is) in input to said at least one PCM/PWM converter (2, 3, 20, 30) by the power in base two of the number of bits (P, S) of said PCM digital signals (Ip, Is) in input to at least one PCM/PWM converter (2, 3, 20, 30), said at least one PCM/PWM converter (2, 3, 20, 30) is a double ramp type, said counter (up-down counter) being fed by said clock signal (E) and being the up/down type, having in input a ramp inversion signal (D) and generating in output a digital comparison signal (Z) composed of the number of bits (P, S) of said PCM digital signals (Ip, Is) in input to at least one PCM/PWM converter (2, 3, 20, 30) in the form of a succession of up and down ramps at a halved frequency (Fin*k/2) compared to the frequency of the PCM digital signals (Ip, Is) in input to said at least one PCM/PWM converter (2, 3, 20, 30), and **characterized in that** it foresees two identical power amplification final stages (101, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input (-) of said two final stages (101, 012) is made by duplicating said at least one PCM/PWM double ramp converter (2, 3) and inverting the ramp inversion signal (D) of said at least one PCM/PWM converter (2, 3) and feeding both said at least one PCM/PWM converter (2, 3) and its duplicate (20, 30) with the same PCM input digital signals (Ip, Is).

12. Amplifier according to claim 4, **characterized in that** said at least one clock generator (5) produces a clock signal (E) whose frequency (Fclock) equals the product of the frequency (Fin*k) of the bits of the PCM digital signals (Ip, Is) in input to said at least one PCM/PWM converter (2, 3, 20, 30) by the power in base two of the number of bits (P, S) of said PCM digital signals (Ip, Is) in input to at least one PCM/PWM converter (2, 3, 20, 30), said at least one PCM/PWM converter (2, 3, 20, 30) being double ramp type, said counter (up-down counter) being fed by said clock signal (E) and being the up/down type, having in input a ramp inversion signal (D) and generating in output a digital comparison signal (Z) composed of the number of bits (P, S) of said PCM digital signals (Ip, Is) in input to at least one PCM/PWM converter (2, 3, 20, 30) in the form of a succession of up and down ramps at a halved frequency (Fin*k/2) compared to the frequency of the PCM digital signals (Ip, Is) in input to said at least one PCM/PWM converter (2, 3, 20, 30), and **characterized in that** it foresees two identical power amplification final stages (101, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input (-) of said two final stages (101, 102) is made by duplicating said couple of PCM/PWM double ramp converters (2, 3) and inverting the signal of ramp inversion (D) of said couple of PCM/PWM converters (2, 3) and feeding both said couple of PCM/PWM converters (2, 3) and their duplicate (20, 30) with the same PCM digital signals (Ip, Is) of said first bus and of said second bus.

13. Amplifier according to claim 12, **characterized in that** it comprises means for inverting the PWM signals (Os, Osn) produced at the output of the PCM/PWM converters (3, 30) of said couple (2, 3) and its duplicate (20, 30) which are fed with said PCM digital signals (Is) containing the less significant bits (LSB), means for attenuating (200) the inverted PWM signals and means for summing each of said PWM signals inverted and attenuated on the inverting node (-) on which the PWM signals produced by the PCM/PWM converters (2, 20) belonging to the other one between said couple (2, 3) of converters or its duplicate (20, 30) are summed.

14. Amplifier according to claim 1, **characterized in that** said oscillator (7) comprises inverters each formed by a couple of MOS transistors (M1, M2; M3, M4; M5, M6) and placed in series and in a loop so that the input of the first of said inverters is connected with the output of the last of said inverters, capacities (C1, C2, C3) in a number equal to that of the inverters and each one having a terminal connected to a respective input of each inverter and the other terminal grounded, a transistor MOS (Mr) having in input said reset pulses (IR) and the output connected to the input of said first inverter.

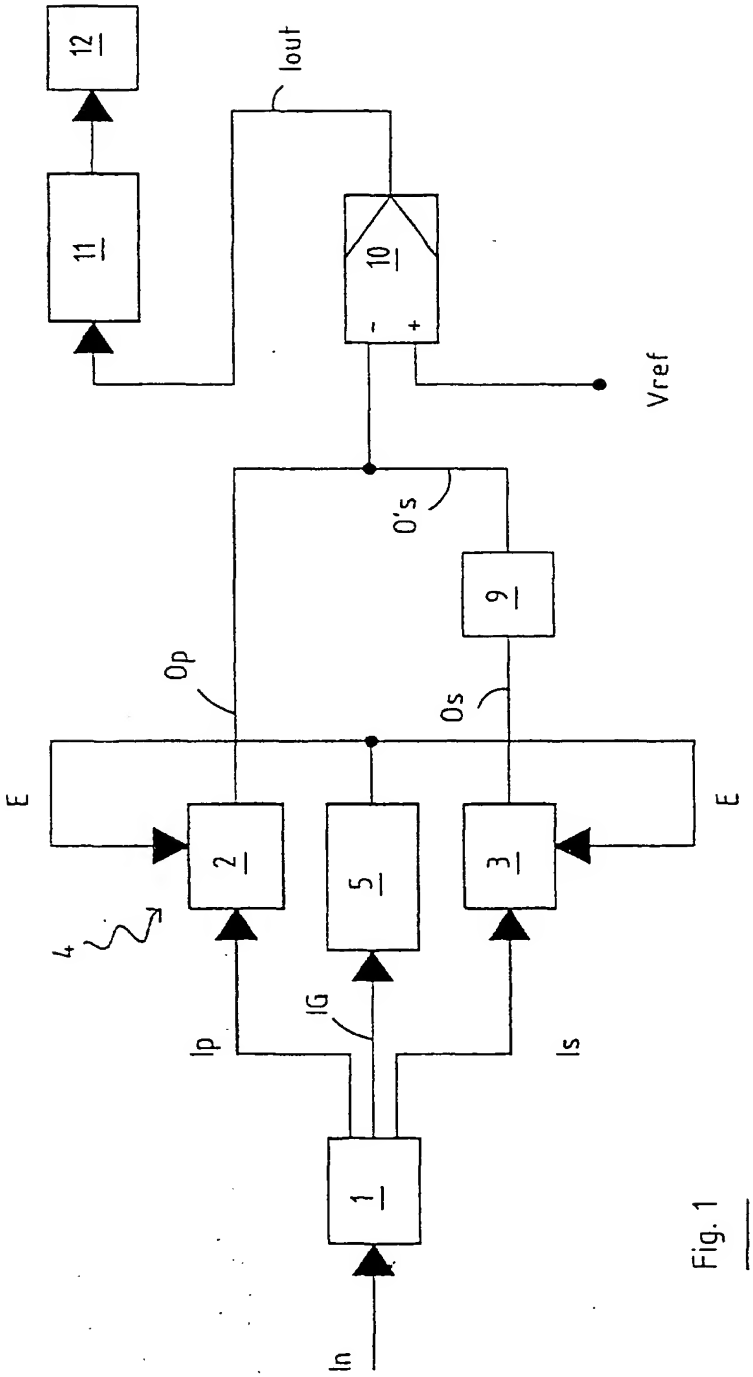

Fig. 1

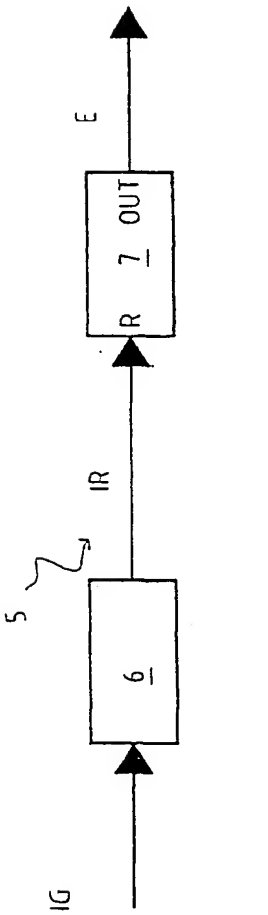

Fig. 2

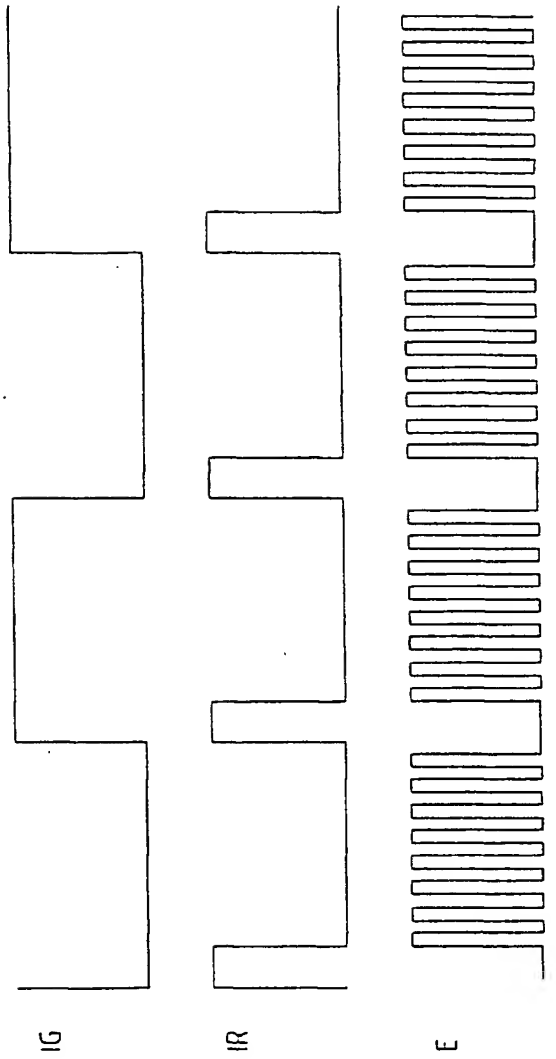

Fig. 3

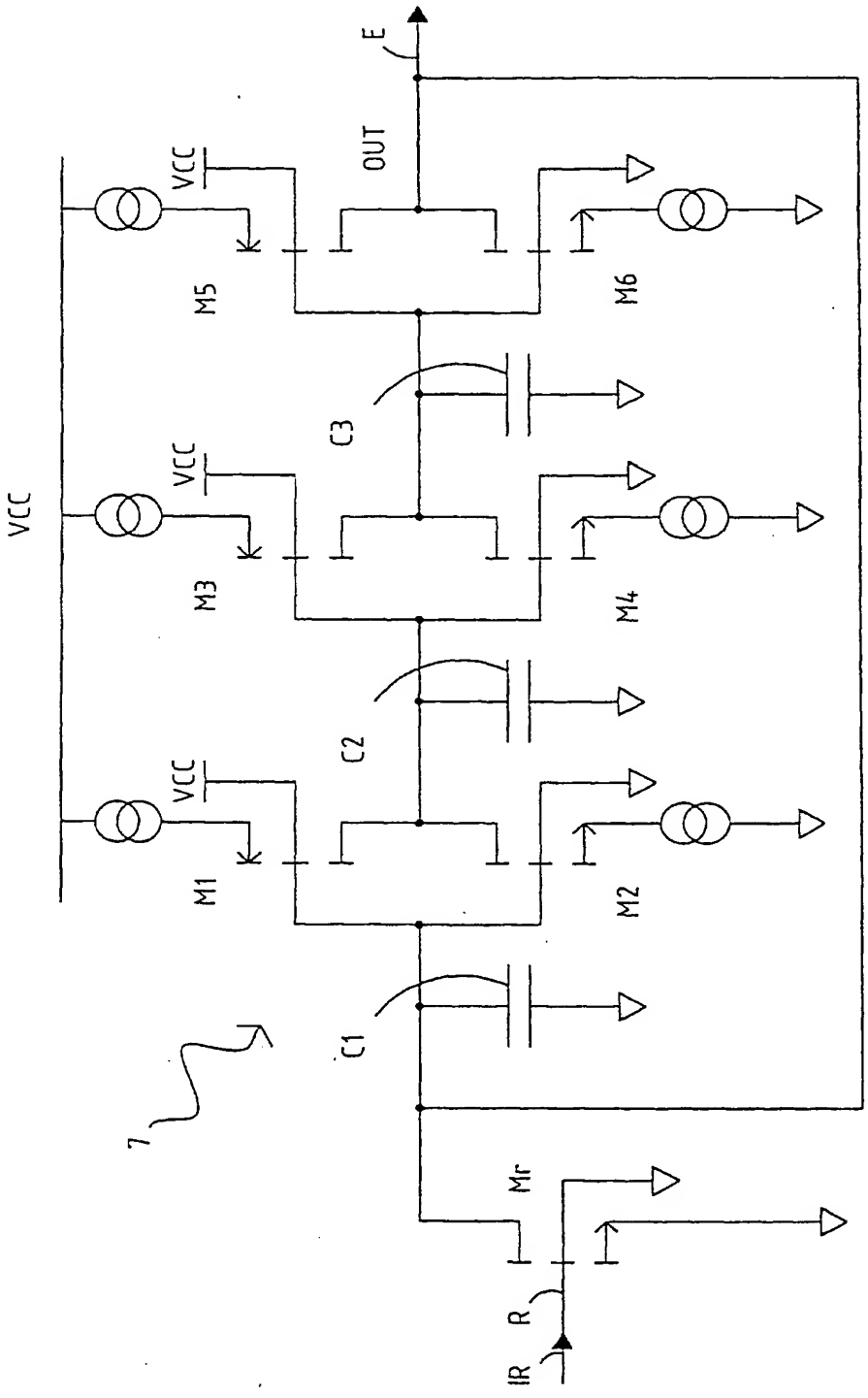

Fig. 4

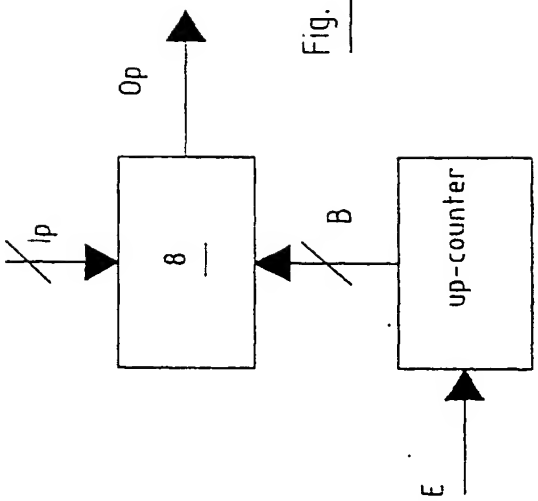

Fig. 5

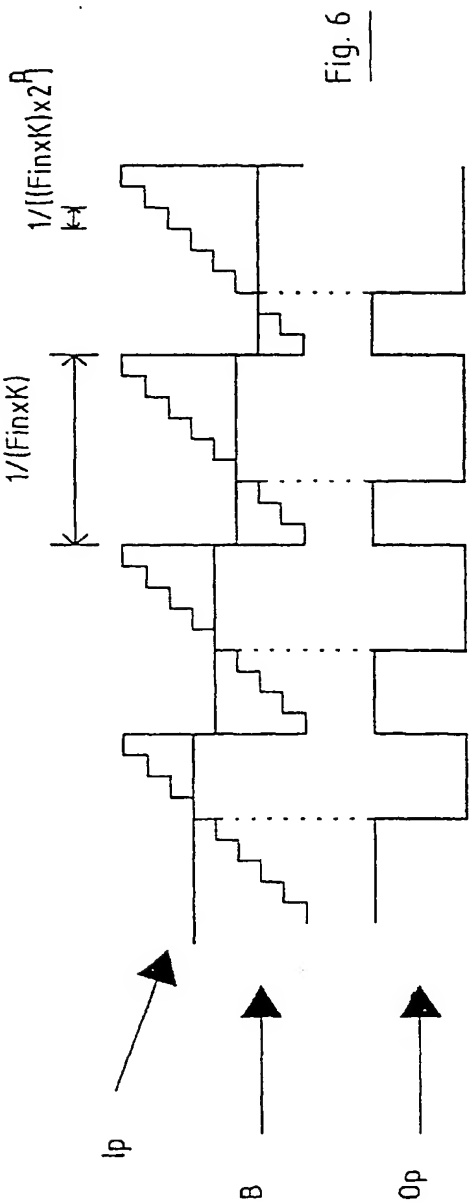

Fig. 6

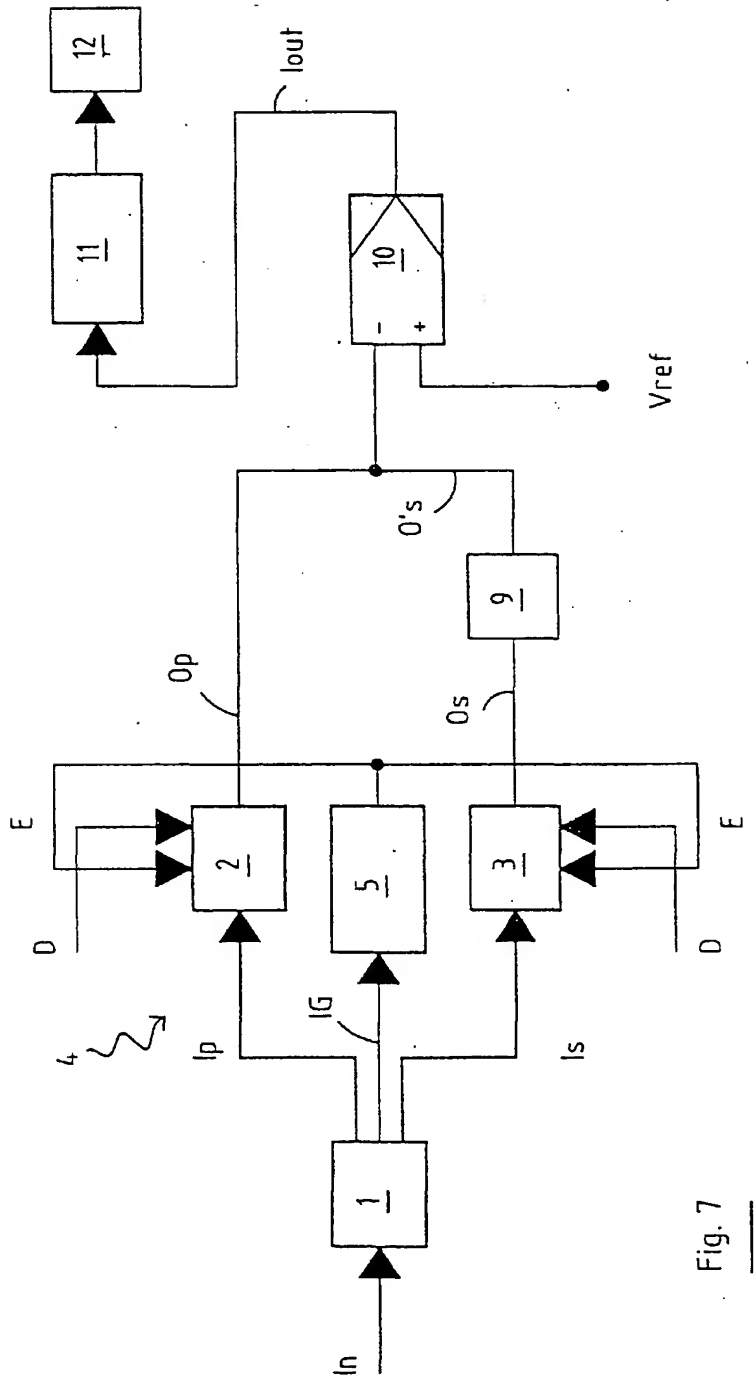

Fig. 7

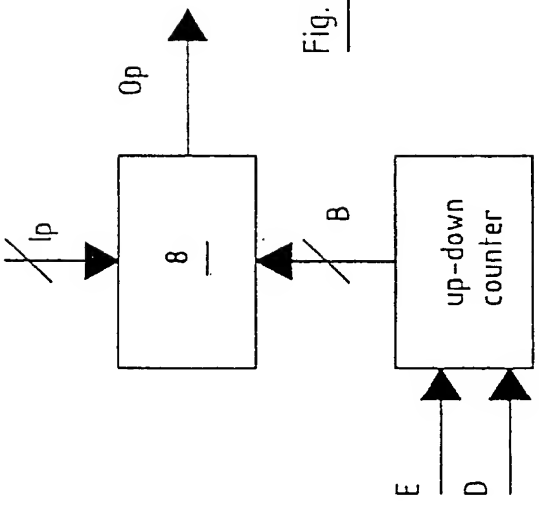

Fig. 8

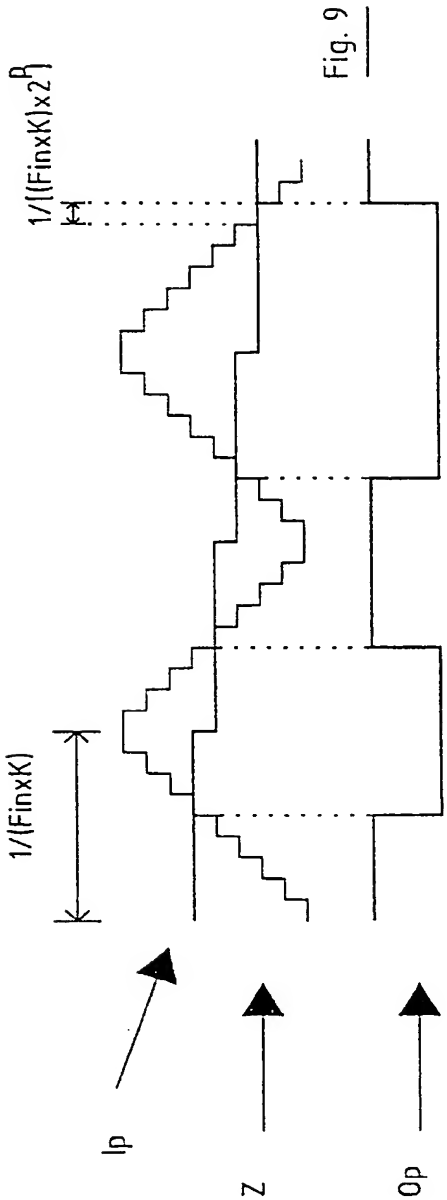

Fig. 9

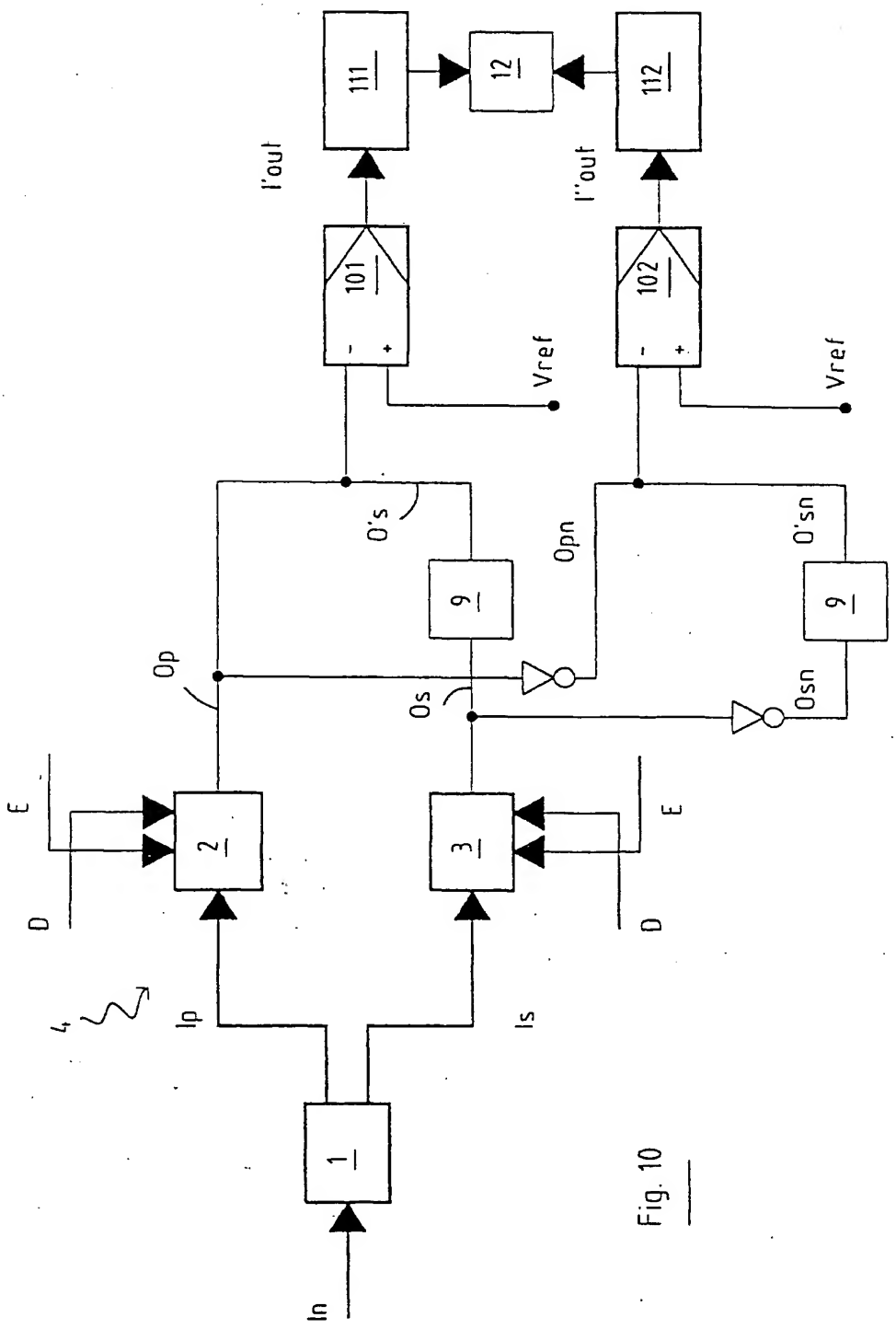
111
12
112
I'out
I''out
101
102
Vref
Vref
O's
Opn
O'sn
9
9
Op
Os
Osn
E
E
2
3
D
D
4
Ip
Is
1
In

Fig. 10

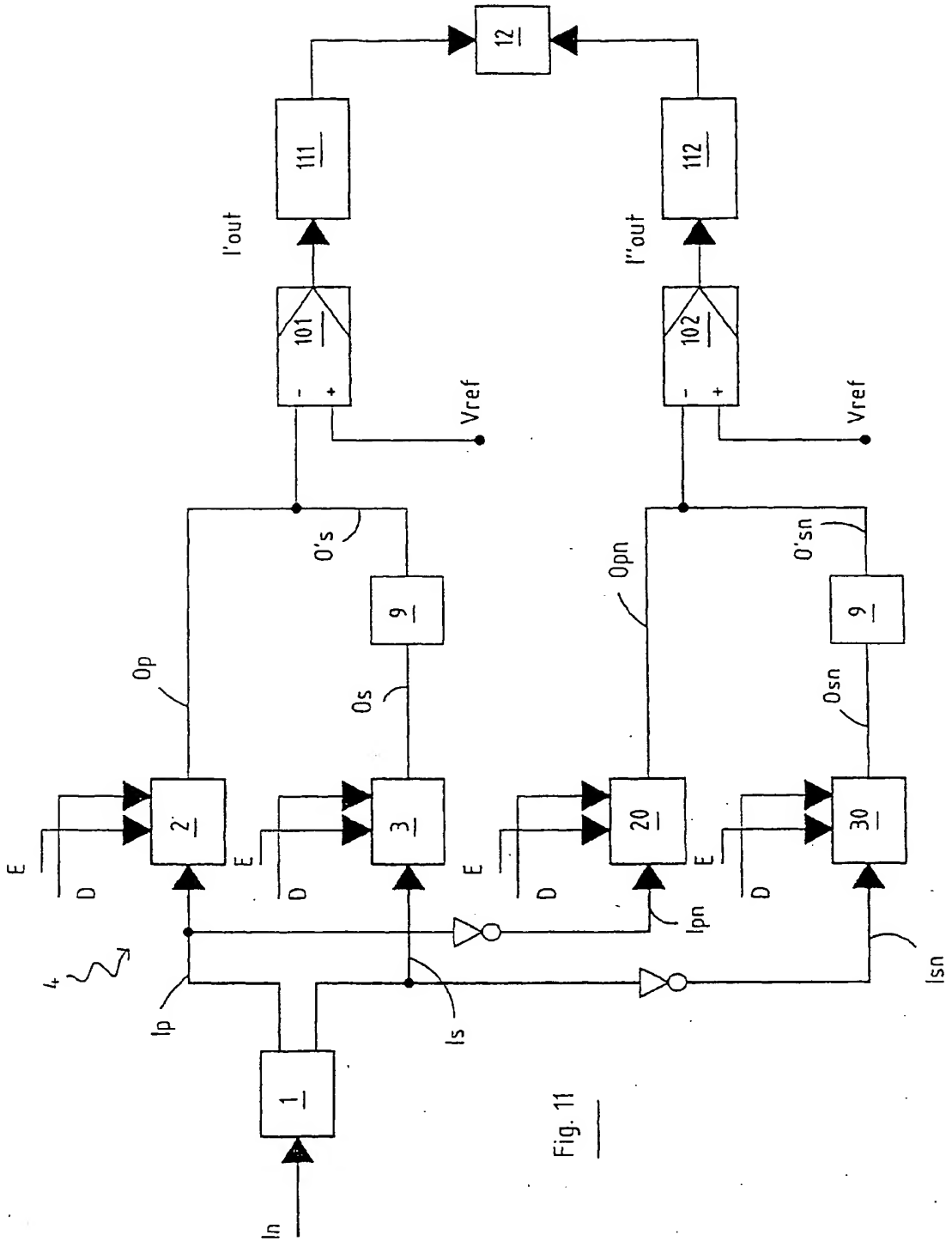
12
111
112
I'out
I''out
101
102
Vref
Vref
O's
O'sn
Opn
9
9
Op
Os
Osn
2'
3
20
30
E
D
E
D
E
D
E
D
Ipn
Isn
Ip
Is
1
In

Fig. 11

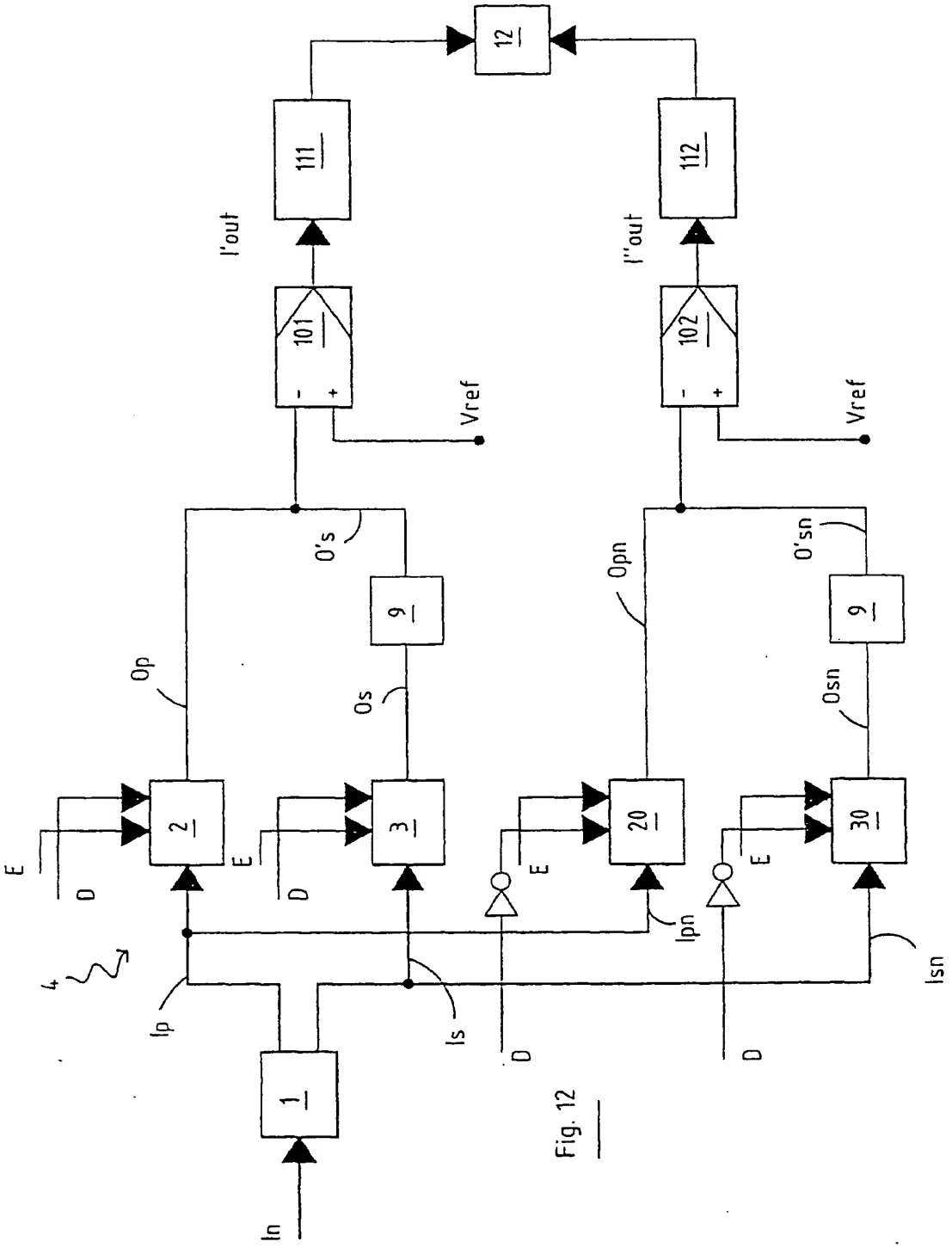
12
111
112
I'out
I''out
101
102
Vref
Vref
O's
O'sn
Opn
9
9
Op
Os
Osn
2
3
20
30
E
D
E
D
E
E
Ipn
Isn
4
Ip
Is
D
D
1
In

Fig. 12

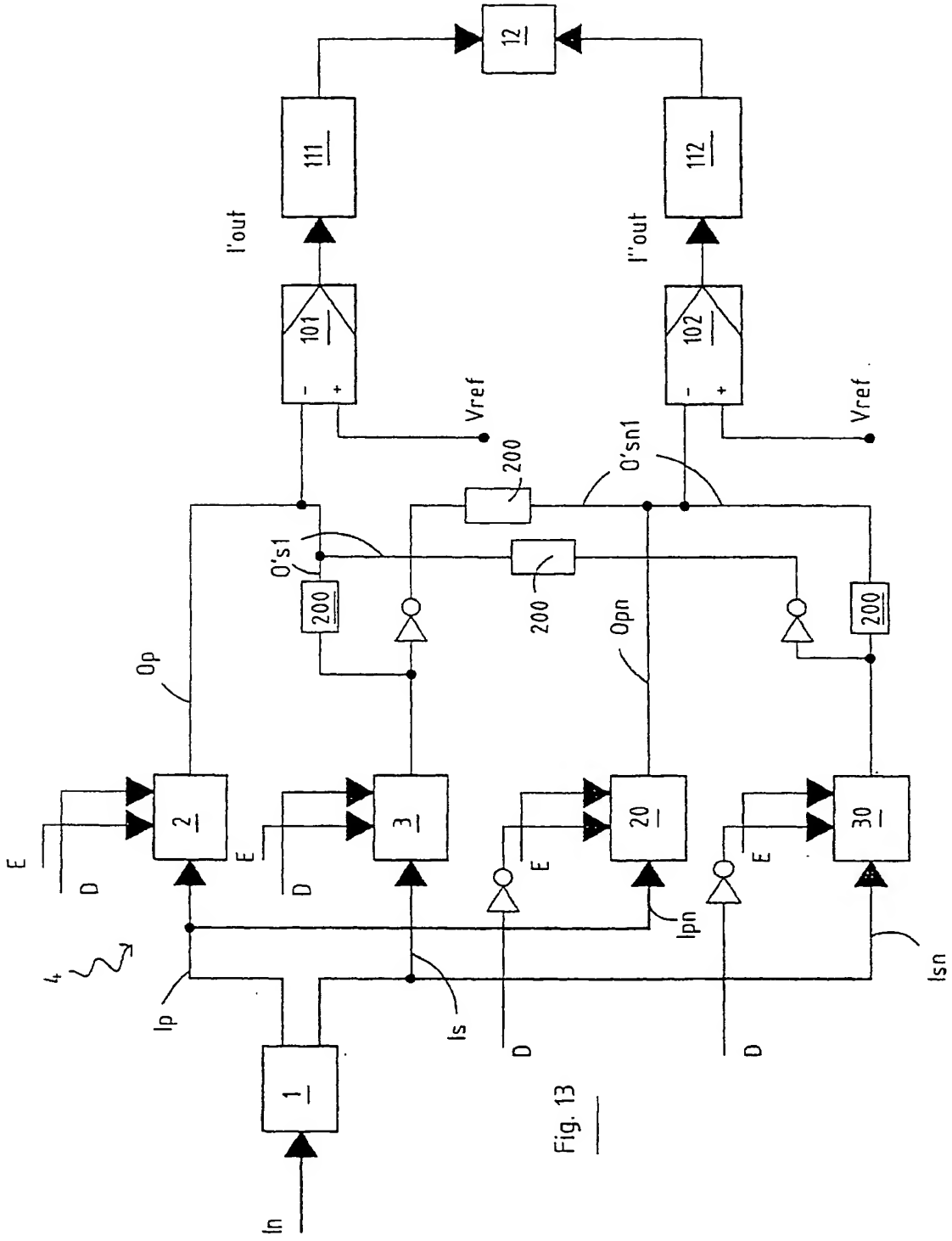
12
111
112
I'out
I''out
101
102
Vref
Vref
200
O'sn1
O's1
200
200
200
Op
Opn
E
D
2
3
20
30
Ipn
Isn
Ip
Is
4
1
In
D
D

Fig. 13

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0560

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	WO 00 35095 A (KONINKL PHILIPS ELECTRONICS NV) 15 June 2000 (2000-06-15) * figures 1,2 *	1,3,6	G06F1/025 H03L7/00 H03M1/68 //H03M1/82
A	US 6 066 988 A (IGURA HIROYUKI) 23 May 2000 (2000-05-23) * figures 4,7,8 *	1	
A	EP 0 711 036 A (MITSUBISHI ELECTRIC CORP) 8 May 1996 (1996-05-08) * figures 5,7,9 *	1	
A	EP 0 457 496 A (SONY CORP) 21 November 1991 (1991-11-21) * figures 3,6 *	1,2	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03M
G06F
H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 January 2001	Verhoof, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 83 0560

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

26-01-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 0035095 A	15-06-2000	NONE	
US 6066988 A	23-05-2000	JP 11068559 A	09-03-1999
EP 0711036 A	08-05-1996	JP 8139577 A	31-05-1996
		DE 69502071 D	20-05-1998
		DE 69502071 T	27-08-1998
		KR 159213 B	20-03-1999
		US 5708381 A	13-01-1998
EP 0457496 A	21-11-1991	JP 4021215 A	24-01-1992
		DE 69128300 D	15-01-1998
		DE 69128300 T	09-04-1998
		US 5148168 A	15-09-1992

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82